Designing of ATM using High Speed Cam

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Abstract— *ATM (Asynchronous Transfer Mode) is a cell-switching and multiplexing technology that combines the benefits of circuit switching (guaranteed capacity and constant transmission delay) with those of packet switching (flexibility and efficiency for intermittent traffic). It provides scalable bandwidth from a few megabits per second (Mbps) to many gigabits per second (Gbps). Because of its asynchronous nature, ATM is more efficient than synchronous technologies, such as time-division multiplexing (TDM).*

With TDM, each user is assigned to a time slot, and no other station can send in that time slot. If a station has a lot of data to send, it can send only when its time slot comes up, even if all other time slots are empty. If, however, a station has nothing to transmit when its time slot comes up, the time slot is sent empty and is wasted. Because ATM is asynchronous, time slots are available on demand with information identifying the source of the transmission contained in the header of each ATM cell.

I. INTRODUCTION

ATM is an International Telecommunication Union–Telecommunication Standardization Sector (ITU-T) standard for cell relay wherein information for multiple service types, such as voice, video, or data, is conveyed in small, fixed-size cells. ATM networks are connection oriented, high-speed, low-delay switching and transmission technology that use short and fixed-size packets called cells to transport information. The maximum time required to translate a VPI/VCI pair increases with the length of the linked list. In a worst case scenario, the allowable time can be exceeded, unless the switch's processor devotes resources to modification of the hashing function in response to changing active VPI/VCI values.

The best approach uses a Content–Addressable Memory (CAM). The CAM turns the normal memory access "inside out". A datum is applied to the CAM, and it outputs the address where a matching value is stored. Therefore, if 4K connections need to be active in a switch, their VPI/VCI values can be stored in a 4K x 28 CAM. The 12 bit address output can be used as an index into a RAM table where the translated VPI/VCIs are stored. While the CAM–based solution is simple, deterministic, and unrestricted, it has been relatively expensive.

CONTENT ADDRESSABLE MEMORY

A CAM has a number of benefits including, CAM entries are structured in parallel so that it can associate the input (comparand) with their memory contents in one clock cycle, CAM's are configurable in multiple formats of width and depth, CAM can be cascaded to increase the size of lookup tables that they can store, provides one of the appropriate solutions for higher speeds. However, the full parallel search operation leads to critical challenges in designing a low-power system for high-speed CAMs. CAMs are power hungry due to the high switching activity of the SL's and ML. A huge surge-on current (i.e., peak current) occurs at the beginning of the search operation due to the concurrent evaluation of the ML which may cause a serious IR drop on the power grid, thus affecting the operational reliability of the chip. As a result, numerous efforts have been put forth to reduce both the peak and the total dynamic power. CAM has three operation modes: READ, WRITE and COMPARE among which "COMPARE" is the main operation as CAM rarely reads or writes. Content addressable memories simultaneously compare an input word to all the contents of memory and return the address of matching locations. This kind of memory provides a distinct speed advantage over RAM in systems requiring quick address comparison or retrieval. CAMs have a single clock cycle throughput making them faster than other hardware- and software-based search systems.

In this work, a parity-bit is introduced to boost the search speed of the parallel CAM with less than 1% power and area overhead. Concurrently, a power-gated ML sense amplifier is proposed to improve the performance of the CAM comparison in terms of power and robustness. It also reduces the peak turn-on current at the beginning of each cycle

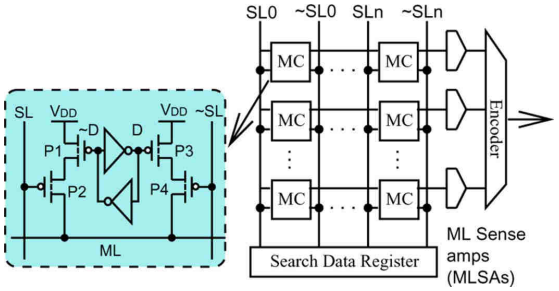

Fig:1 Block diagram of a Conventional CAM

II. INTRODUCTION OF A PARITY BIT

To enhance the speed by reducing delay a parity-bit is introduced to boost the search speed of a CAM. Concurrently, a power-gated ML sense amplifier is added to improve the performance of the CAM's ML comparison in terms of power and robustness and also reduces the peak turn-on current at the beginning of each search cycle.

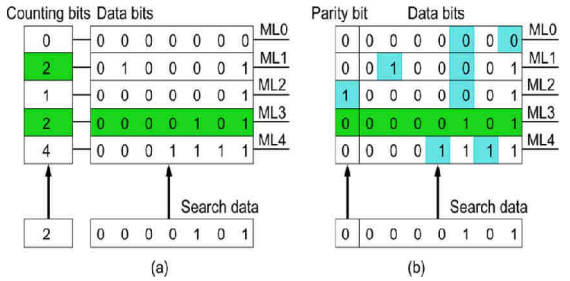

Fig:2 Conceptual View of (a) conventional CAM, (b) parity based CAM

The introduced auxillary bit looks similar with the existing data bit but in operating principle, it totally differs. Here we have the discussions about pre computation scheme as well as parity bit based scheme

a) PRE COMPUTATION CAM

The pre-computation CAM uses a additional bits to filter some mismatched CAM words before the actual comparison. These extra bits are derived from the data bits and are used as the first comparison stage. For example, in Fig. 2(a) number of "1" in the stored words are counted and kept in the counting bits segment. When a search operation starts, number of "1"s in the search word is counted and stored to the segment on the left of Fig. 2(a). These extra information are compared first and only those that have the same number of "1"s are turned on in the second sensing stage for further comparison. This scheme reduces a significant amount of power which is required for data comparison statistically.

The main design idea is to use additional silicon area and search delay to reduce energy consumption. All existing designs shares one similar property. The ML sense amplifier essentially has to distinguish between the matched ML and the 1-mismatch ML. This makes CAM designs sooner or latter face challenges since the driving strength of the single turned-on path is getting weaker after each process generation while the leakage is getting stronger. This problem is usually referred to as Ion/Ioff . Thus, we propose a new auxiliary bit that can concurrently boost the sensing speed of the match line and at the same time improve the ML Ion/Ioff of the CAM by two times.

b) PARITY BIT BASED CAM

The parity bit based CAM design is shown in Fig. 2(b) consisting of the original data segment and an extra one-bit segment, derived from the actual data bits. We only obtain the parity bit, i.e., odd or even number of "1"s. The obtained parity bit is placed directly to the corresponding word and ML Thus the new architecture has the same interface as the conventional CAM with one extra bit. During the search operation, there is only one single stage as in conventional CAM. Hence, the use of this parity bits does not improve the power performance. However, this additional parity bit, in theory, reduces the sensing delay and boosts the driving strength of the 1-mismatch case (which is the worst case) by half, as discussed below.

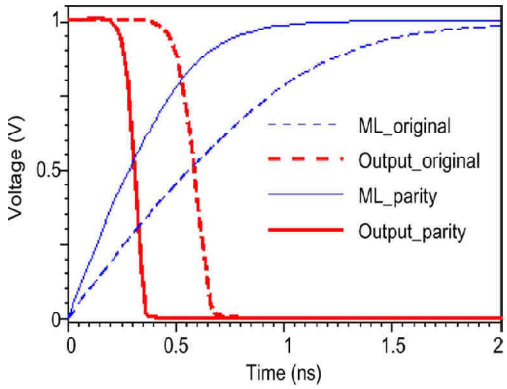

Fig 3 Comparision graph of existing and proposed architecture with 1 mismatch

In the case of a matched in the data segment, the parity bits of the search and the stored word is the same, thus the overall word returns a match. When 1 mismatch occurs in the data segment, numbers of "1"s in the stored and search word must be different by 1. As a result, the corresponding parity bits are different. Therefore now we have two mismatches (one from the parity bit and one from the data bits). If there are two mismatches in the data segment, the parity bits are the same and overall we have two mismatches. With more mismatches, we can ignore these cases as they are not crucial cases. The sense amplifier now only have to identify between the 2-mismatch cases and the matched cases. Since the driving capability of the 2-mismatch word is twice as strong as that of the 1-mismatch word, the proposed design greatly improves the search speed and the Ion/Ioff ratio of the design. Fig. 3 shows the 1-mismatch ML transient waveforms of the original and the proposed architecture during the search operation.

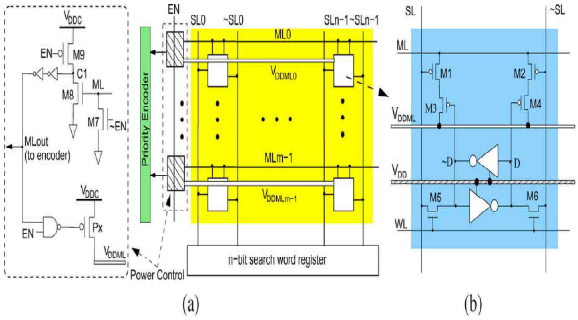

Fig: 4 Proposed CAM

III. GATED-POWER ML SENSE AMPLIFIER

The proposed CAM architecture is depicted in Fig. 4. The CAM cells are organized into rows (word) and columns (bit). Each cell has the same number of transistors as the conventional P-type NOR CAM and use a similar ML structure. However, the "COMPARISON" unit, i.e., transistors M1-M4, and the "SRAM" unit, i.e., the cross-coupled inverters, are powered by two separate metal rails, namely VDDML and the VDD, respectively. The VDDML is independently controlled by a power transistor Px and a feedback loop that can auto turn-off the ML current to save power.

The purpose of having two separate power rails of (VDDML and VDD) is to completely isolate the SRAM cell from any possibility of power disturbances during COMPARE cycle. The gated-power transistor Px, is controlled by a feedback loop, denoted as "Power Control" which will automatically turn off Px once the voltage on the ML reaches a certain threshold. At the beginning of each cycle, the ML is first initialized by a global control signal EN. At this time, signal EN is set to low and the power transistor Px is turned Off . This will make the signal ML and C1 initialized to ground and VDD , respectively. After that, signal EN turns *HIGH* and initiates the COMPARE phase. If one or more mismatches happen in the CAM cells, the ML will be charged up.

Interestingly, all the cells of a row will share the limited current offered by the transistor Px, despite whatever number of mismatches. When the voltage of the ML reaches the threshold voltage of transistor M8, voltage at node C1 will be pulled down. After a certain but very minor delay, the NAND2 gate will be toggled and thus the power transistor Px is turned off again. As a result, the ML is not fully charged to VDD, but limited to some voltage slightly above the threshold voltage of M8. One can see that, the slopes of the ML , node C1 and node MLOUT depend on the number of mismatches. When more mismatches happen the ML and node C1 change faster. Less number of mismatches will slow down the transition of node C1 and results in a longer delay to turn off transistor Px. The voltage on the ML is finally charged to only around 0.5 V which is far below VDD and hence the power consumption is reduced.

With the introduction of the power transistor Px, the driving strength of the 1-mismatch case is about 10% weaker than that of the conventional design and thus slower. However, as we combine this sense amplifier with the parity bit scheme, the overall search delay is improved by 39%. Thus the new CAM architecture offers both low-power and high-speed operation.

IV. CAM IN ATM SWITCH

Content addressable memory (CAM) can accelerate the performance of any application that requires faster searches of its databases, lists, or patterns. A CAM application example is in the Asynchronous Transfer Mode (ATM) switching networks. CAM can be used to accelerate VCI/VPI translation tables in ATM switching networks.

The ATM switch is a high-speed device that uses packet switching techniques in public networks and is capable of supporting many classes of traffic, such as data, video, and voice. ATM traffic consists of a series of fixed-length packets called "cells." Each cell has a 5-byte fixed length header and a 48-byte payload.

ATM networks, which are connection-oriented devices, need a virtual circuit (VC) to be set up across the network prior to any data transfer. Two types of circuits include the virtual path (VP), which is identified by a virtual path identifier (VPI), and the channel path, which is identified by the virtual channel identifier (VCI).

Virtual path connection (VPC) is used to route multiple virtual channels through an ATM network, and virtual channel connection (VCC) is a bidirectional facility to transfer ATM traffic between layers.

Because VCI/VPI values are localized, each segment of the connection has a unique VPI/VCI combination. When a cell travels through the network from the user network interface (UNI) through the switch to the network node interface (NNI), the VPI/VCI value is changed to the value the next segment of connection uses through a process called a VPI/VCI translation, shown in Fig 3.6. The time required to compute VPI/VCI translations is critical in order to determine the performance of ATM networks. CAM can act as an address translator for look-up tables (LUTs) in ATM switches and perform VPI/VCI translation quickly. VPI/VCI fields from the ATM controller are compared against a list of current connections stored in the CAM array. CAM generates an address that is used to access an embedded RAM, where

VPI/VCI mapping data and other connection information are stored. VPI/VCI data from RAM is added on to the cell and sent to the switch.

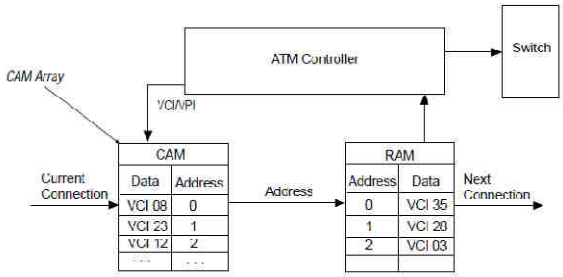

Fig. CAM in ATM switch

V. PERFORMANCE COMPARISONS

In this section, performance of the proposed design will be evaluated using the conventional circuit as references. The power consumption is limited by the amount of charge injected to the ML at the beginning of the search. A similar concept is utilized with a positive feedback loop to boost the sensing speed. Both designs are very power efficient.

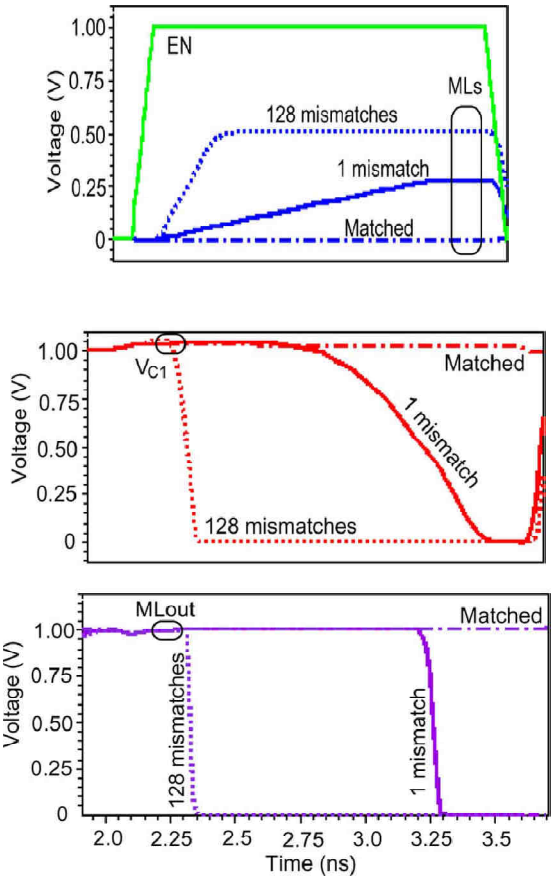

Fig 5 Waveforms of some important nodes during evaluation of three rows of 128-bit of the proposed design

a) Peak Current and IR Drop Attenuation

The proposed power controller demonstrates a great reduction in the transient peak current. The conventional design's peak current increases almost linearly from 25 µA(1 mismatch) to 1.45 mA (64 mismatches) and finally 2.8 mA (128mismatches). Although the overall transient ML charge up current ofthe proposed design also increases with the number of mismatches, it will soon reach its limit due to the presence of the gated-power transistor Px. For instance, when 128 mismatches occurs, the peak current is capped at 155 µA, which is less than eight times as compared to the case when only one mismatch occurs (i.e., 21 µA). This drastic reduction in the peak current translates to a vast improvement in operation reliability.

b) Dynamic Power Consumption

Because the power-gated transistor is turned off after the output is obtained at the sense amplifier, the proposed technique renders a lower average power consumption. This is mainly due to the reduced voltage swing on the ML bus. Another contributing factor to the reduced average power consumption is that the new design does not need to precharge the SL buses because the EN signal turns off transistor Px of each row and hence the SL buses do not need to be pre-charged, which in turn saves 50% power on the SL buses.

c) Process Variation Analysis

Process variation is a critical issue in nano-scale CMOS technologies. We simulate the performance of the proposed design against empirical process variation data from the foundry. It is worth mentioning here that the feedback loop to turn off the gated-power transistor Px operates digitally and hence is almost insensitive to process variations. Similar to the conventional design, there are two scenarios where the proposed design may sense the results wrongly: 1) the sense amplifier is enabled too early, the 1-mismatch ML has not been pulled up to a voltage higher than the threshold value and thus trigger the output inverter and 2) the delay of the enable signal is too long, resulting in the matched ML to be pulled up by the leakage current, indicating wrong miss. We use 50000-cycle Monte Carlo simulations on these designs at different supply voltages and count the number of errors accordingly. They are very sensitive to process variations with more than 1000 and 10,000 errors count, respectively. Also, they stop working at 0.9 V supply. On

the contrary, the proposed and the conventional design has no sensing error even if VDD scales down to 0.7 V. At lower supply voltage, the conventional design continues to work 100% correctly while the proposed design has 51 and 298 error counts at 0.6 and 0.5 V, respectively. This is because both designs operates at the same frequency but the proposed design has a smaller pull-up current due to the gated-power transistor Px and hence some times error happens. We have carried out a separate simulation for the proposed design with a slightly slower frequency and has confirmed that no error occurs

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VI. CONCLUSION

An effective parity-bit based search operation that offers several major advantages namely reduced peak current (and thus IR drop), average power consumption (28%), boosted search speed (39%), minimization of gate count and improved process variation tolerance is implemented.
Parity bit technique when applied in ATM switching allocates less power to match decisions involving a larger number of mismatched bits. It is much more stable than previous designs while maintain their low-power consumption property. At 1 V operating condition, the design is stable with no sensing errors. The improvement in search speed indicates that ATM switches can be replaced by CAM in order to perform address translation in a faster mode.

VII. FUTURE ENHANCEMENTS

Future CAM is a part of Spintronics logic integrated circuit technology that utilize the negative properties of electrons together with the spin magnetic moment. The future CAM utilizes the vertical magnetization of vertical domain wall elements in reaction to magnetic substances in order to enable data that is processing within the CAM to be stored on a circuit without using power. This contrasts to conventional technologies that required data to be stored within memory. As a result, data can be saved on circuits even when power is cut from the CAM.
Use of this CAM in combination with existing nonvolatile memory is related to greater non-volatility of CPU for electronics and other storage devices. Furthermore, use of this new CAM may enable the development of electronics that start instantly and consume zero electricity while in standby mode.
In order for a CAM to be both nonvolatile and maintain a high speed, two spintronics devices, spinning in opposite directions to one another, were connected within the same cell. In terms of constructing the circuit, writing is done once by connecting two devices in a series using recently developed three pin particles that separate the current path into writing and reading.
In addition to the vertical domain wall element can connect in series by separating the route of current into reading and writing, the newly developed CAM circuit technologies can reduce the number of transistors from eight to three in every two cells by sharing transistors. This results in a 50 % of area reduction.

REFERENCES

[1] A. T. Do, S. S. Chen, Z. H. Kong, and K. S. Yeo, “A low-power CAM with efficient power and delay trade-off,” in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), 2011, pp. 2573–2576.
[2] I.Arsovski and A. Sheikholeslami “A mismatch-dependent power allocation technique for match-line sensing in content-addressable memories,” IEEE J. Solid State Circuits, vol. 38, no. 11, pp. 1958–1966, Nov. 2003.
[3] K. Pagiamtzis and A. Sheikholeslami, “A low-power content-addressable memory (CAM) using pipelined hierarchical search scheme,” IEEE J. Solid-State Circuits, vol. 39, no. 9, pp. 1512–1519, Sep. 2004.
[4] K. Pagiamtzis and A. Sheikholeslami “Content-addressable memory (CAM) circuits and architectures:A tutorial and survey,” IEEE J. Solid-State Circuits, vol. 41, no. 3, pp. 712–727, Mar. 2006.
[5] N. Mohan, W. Fung, D. Wright, and M. Sachdev, “A low-power ternary CAM with positive-feedback match-line sense amplifiers,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 56, no. 3, pp. 566–573, Mar. 2009.
[6] N. Mohan and M. Sachdev, “Low-leakage storage cells for ternary content addressable memories,” IEEE Trans. Very Large Scale Integer.(VLSI) Syst., vol. 17, no. 5, pp. 604–612, May 2009.
[7] O. Tyshchenko and A. Sheikholeslami, “Match sensing using match linestability in content addressable memory (CAM),” IEEE J. Solid- State Circuits, vol. 43, no. 9, pp. 1972–1981, Sep. 2008.
[8] S. Baeg, “Low-power ternary content-addressable memory designusing a segmented match line,” IEEE Trans. Circuits Syst. I, Reg.Papers, vol. 55, no. 6, pp. 1485–1494, Jul. 2008.